A 900 MHz / 2.45 GHz RF Frontend
For Passive RFID Transponders

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Abstract—The RF frontend is one of the key elements in passive transponders, accounting for such diverse operations as RF-DC conversion, voltage regulation, modulation and demodulation of the incident RF wave. In this paper, the design of a high-performance frontend for passive RFID transponders under the international standard ISO/IEC 18000-4/6 is presented. Its physical implementation has been carried out on a commercial RF-CMOS 0.35µm technology. Special structures presented. Its physical implementation has been carried out on a commercial RF-CMOS 0.35µm technology. Special structures such as Schottky diodes and MIM capacitors are not necessary. The frontend provides a regulated supply voltage of 1V at a nominal current consumption of 2µA for the transponder back-end (the digital core and additional analog circuits such as an on-chip temperature sensor). The chip is matched to a specially designed resonant antenna. Measurement results coincide largely with those obtained through simulation, thus confirming the effectiveness of the design procedure. A maximum read-out distance of up to 5.1 m is achieved at UHF frequency band under European regulations. The front end can also operate in the microwave frequency band (2.45GHz) with a reduced read out distance.

Index Terms—Passive, UHF, microwave, RFID, RF frontend, transponder

I. INTRODUCTION

RFID as a prospective automatic identification technology is being applied to a wide variety of fields [1] [2]. In a RFID system, the tags storing data and communicating with a base station or reader can be attached to or incorporated into products, animals and persons. A typical RFID system consists of a reader and a transponder; the latter has in general an antenna, an analog RF-frontend and a digital IC core. The transponder itself can be completely passive [3][4][5], semi-passive [6], or active. Sometimes sensors are also included. The passive RFID tag obtains its power from the interrogating electromagnetic signal generated by the reader and requires thus no battery.

The analog frontend is the key circuit of the passive RFID transponder. It rectifies the incoming RF signal providing a stable regulated voltage supply for the digital core and other circuits. Furthermore, in receiving mode, it detects and demodulates the ASK modulated RF signal and provides a digital bitstream for the digital core. In transmitting mode, it changes the input impedance of the transponder between two states in order to realize the backscatter modulation. In addition, it generates the power-on-reset signal that resets the digital core during power-up.

For correct tag operation at the longest possible readout distance, the RF to DC conversion efficiency must be optimized in first place. Schottky diodes, which have low forward voltage and quick transition time, are frequently employed in the RFID frontend [5][7][8]. However, many standard CMOS technologies do not provide a HF-Schottky diode. Some researchers use diode-connected MOS transistor to replace this type of diodes [9], demanding in turn low-threshold transistors. Otherwise, the RF-DC conversion efficiency decreases drastically. A further consideration to increase the readout distance is to carefully design all functional blocks as to minimize the overall power consumption.

This paper describes the design of an analog frontend for passive UHF/microwave RFID (Radio Frequency Identification) transponders under the international standard ISO/IEC 18000-4/6. The rectifier proposed in [10] is used for the RF to DC conversion. The conversion efficiency is comparatively high with no need of low-threshold MOS transistors or HF-Schottky diodes. In addition, the voltage reference and amplifiers operate in weak inversion region, greatly reducing the power consumption. The bias current is limited to 100nA. The chip itself is connected to a matching antenna fabricated on a PCB. Measurement results are also presented showing that such a frontend with the chosen antenna can provide 1V and 2µA for the digital core and other circuits. It can operate at a read out distance of approximately 5.1 m in the UHF frequency band under European RFID regulations.

II. STRUCTURE OF THE ANALOG FRONTEND

The RF-frontend is composed of a rectifier, a charge pump, a modulator, a demodulator, a regulator and a POR (power on reset) circuit, as shown in Fig.1. Ports hf1 and hf2 are connected to the antenna. The port vrddata feeds the modulator with a digital bitstream. vdem is the received data, vreg is the regulated output power supply (1V, 2µA), and vpor the reset signal generated by the Power-On-Reset (POR) circuit.

![Figure 1: Diagram of the RF-backend](image-url)
The passive transponder, as its name implies, has no external battery, obtaining its power directly from the electromagnetic signal. The antenna collects the transmitted power by the reader, inducing a voltage at the input of the rectifier. The rectifier fulfills two tasks: 1) it is the first stage of the RF-DC converter, and 2) it provides the envelope of the RF signal to the demodulator. After rectification, the DC signal with low-frequency ripple is fed to charge pumps, which increase the output voltages \(v_{\text{high}}\) and \(v_{\text{low}}\) even further. These in turn are applied to the low-dropout voltage regulator producing \(v_{\text{reg}}\), which provides the power supply for the digital IC, sensors and other circuits. Increasing the output current will induce a dramatic increase of the power loss in the charge pump. In order to circumvent this problem, we use two charge pumps to up-convert the DC voltage, separating the DC current in two paths and thus reducing the power loss.

During a write operation, the envelope of the ASK modulated RF input signal is demodulated and a digital bitstream is delivered to the digital core \(v_{\text{dem}}\). On the other hand, a read operation takes place when a digital bitstream is delivered to the modulator through the port \(v_{\text{trdata}}\). The modulator changes the input impedance of the transponder, producing a deliberate mismatch between antenna and chip. In this way energy is either absorbed (matched state) or partly reflected (mismatched state).

III. FUNCTIONAL BLOCKS

A. The RF-DC converter

The RF-DC converter consists of a rectifier and two charge pumps, as shown in Fig. 1. The rectifier is based on [10], and is shown in Fig. 2. Note that the MOS transistors act as switches.

![Figure 2: rectifier](image)

The main factors affecting power consumption are the dimension of the transistors, the input voltage peak amplitude, and the required output power. For an output power in the micro-Watt range, the smaller the transistors (0.35µm technology), the lower the power consumption of the rectifier. Therefore, we choose for this design transistors with minimal dimensions. The power consumption of this rectifier also rises with increasing input amplitude \(v_{\text{in}}\). A moderate value of 1.2Vpp is selected. However, in this situation, the output voltage \(v_{\text{rect}}\) is not large enough to drive the rest of the circuits. In order to loose this issue an efficient charge pump was implemented.

Charge pumps 1 and 2 yield the voltages \(v_{\text{high}}\) and \(v_{\text{low}}\), respectively. These circuits are differential versions of the Dickson charge pump where the diodes are replaced by diode-connected n-MOS transistors. The involved capacitors and the number of stages were also optimized. The power consumption of a charge pump depends on the output current at a fixed output voltage. After optimizing the efficiency of the RF-DC converter, the charge pump 2 \(\rightarrow v_{\text{high}}\) is fed by \(v_{\text{rect}}\) in order to alleviate the load of charge pump 1 \(\rightarrow v_{\text{low}}\).

The achieved efficiency of the RF-DC converter operating at 900MHz reaches 18% for the following conditions: \(v_{\text{high}}\) 1.7V, 300nA and \(v_{\text{low}}\) 1.2V, 3.5µA.

B. Regulator

The voltage regulator provides a relatively steady voltage power supply \(v_{\text{reg}}\) and is composed of a low-voltage low-power voltage reference and a low dropout regulator, as shown in Fig.3.

![Figure 3: Regulator](image)

Voltage reference

The voltage reference consists of a startup circuit, a self-biased current mirror and an output stage, as shown in Fig. 4. In order to reduce the power consumption all transistors operate in weak inversion [11].

The current mirror generates a reference current \(I_0\), which is almost independent of the supply voltage \(v_{\text{low}}\). The current \(I_0\) can be calculated as follows: since \(V_{gs2} - V_{gs3} = I_0 R_2\) and MN2 and MN3 work in weak inversion, the gate source voltage of each MOSFET is given by

\[
V_{gs} = \frac{nKT}{q} \ln \frac{I_0}{(W/L)L_\text{inv}}
\]

where \(n = 1 + C_d / C_{gs}\), \(C_d\) is the surface depletion capacitance and \(C_{gs}\) is the gate oxide capacitance. Thus,
In order to let MN2 and MN4 work in weak inversion, $I_0$ is chosen to be approximately 100nA at room temperature. The length of MN2 and MN4 is 10 $\mu$m. In this way, undesired short-channel effects can be effectively suppressed. From Eq. (2), it is seen that $I_0$ is a PTAT (proportional to absolute temperature) magnitude.

Correspondingly, a PTAT current $I_{ref}$ is generated and flows through resistors $R_1$, $R_0$ and the bipolar transistor $Q_0$. $v_{ref}$ is given by

$$v_{ref} = I_{ref} (R_1 + R_0) + V_{be}$$

$R_1$ is a n-well resistor, which has a positive temperature coefficient. $R_0$ is fabricated with a high resistive poly-Si, which has a negative temperature coefficient. On the other hand, the base-emitter voltage of $Q_0$ has a negative temperature coefficient. Aiming at a first order suppression of the temperature dependency, suitable sizes for these three components can be easily selected which minimize the temperature dependence of $v_{ref}$ within the operating temperature range. In this way, a power-supply and temperature quasi independent reference voltage can be obtained with minimal circuit complexity and very low power consumption.

**Low dropout voltage regulator**

As shown in Fig.3, this circuit is made up of an error amplifier (an OTA) and a NMOS pass transistor. The OTA is a two-stage operational transconductance amplifier operating in weak inversion [12]. A large W/L-ratio is chosen for MN0, resulting in a low drain-source voltage drop and thus requiring a relatively low high-side voltage $v_{low}$. However, choosing the W/L-ratio too large will shift a pole to low frequency, reducing the bandwidth. On the other hand, a small W/L-ratio results in a small phase margin and thus ringing and a large settling time.

### C. Demodulator

The demodulator consists of an input stage (MN1, $R_0$, $C_0$), a hysteresis comparator and an output stage (MP0 and MN0), as shown in Fig.5.

**Input stage**

MN1’s drain-source resistance and associated capacitance ($C_0$) make up a low-pass filter. $C_0$ and the comparator input resistance make up a second low-pass filter. The latter has a much large time constant than the former. The average signal $v_{av}$ is generated in this way and is close to the actual average value of the input (ASK modulated) signal $v_{rect}$. The circuits builds a moving average, since the actual average value of $v_{rect}$ may vary with the distance to the reader, thus precluding the use of a constant value. The comparator performs then the comparison between $v_{rect}$ and $v_{av}$, generating a base-band digital signal.

**Hysteresis comparator**

The comparator is shown in Fig 6. The trip point will occur when

$$\frac{I_{MPB}}{I_{MPA}} = \frac{(W/L)_{MPB}}{(W/L)_{MPA}} = \frac{1}{m} \quad \text{or} \quad \frac{I_{MPA}}{I_{MPB}} = \frac{(W/L)_{MPA}}{(W/L)_{MPB}} = m$$

Because the reference current is chosen to be approximately 100nA, the input transistors MN0 and MN4 operate in weak inversion. Therefore, the hysteresis width is given by

$$\Delta V_{IL} = nV_t \ln(m) - nV_t \ln(1/m) = 2nV_t \ln(m)$$

where $n$ is the subthreshold slope factor and $V_t$ is the thermal voltage. The hysteresis width can be controlled by adjusting the value of $m$.

### D. ASK-modulator

The simple ASK-modulator is made up of two NMOS transistors, as shown in Fig.7.

The modulator is connected in parallel to the input of the rectifier. If $v_{trdata}$ is higher than MN0’s threshold voltage $V_r$, the drain-source resistance of these two transistors will be very small, short-circuiting the antenna. If $v_{trdata}$ is lower than $V_r$, the two transistors are turned off and have no influence on the impedance seen by the antenna. Thus, when $v_{trdata}$ changes...
between “1” and “0”, the incident wave is either absorbed or reflected and backscattering takes place.

IV. MEASUREMENT

The frontend has been fabricated on a commercial RF-CMOS 0.35µm technology. The antenna and test circuits for the frontend were implemented on a regular PCB (Substrate: FR4. Cu thickness: 1.6µm). The chip was directly attached to the board using a COB-technique and finally wire-bonded, as depicted in Fig.9. The antenna was designed and simulated considering the bonding parasitics, after measuring the chip input impedance with a true-differential network analyzer.

In order to test the frontend, an antenna (Gain 1.5) was connected to a RF signal generator (Agilent E8257D).

Owing to the restricted output power of the generator (max. 14dBm) and the return loss of the reader antenna (-10dB), the ERP-power can be estimated to be approximately 34mW.

Figure 10 shows the output of the demodulator. The read-out distance under the mentioned conditions is 60cm at 900MHz. Employing eq. (6), the power available to the chip \( P_{av} \) can be calculated.

\[
\begin{align*}
\text{(a) Input RF signal} & \quad \text{(b) } V_{\text{dem}} \quad \text{(c) } V_{\text{stg}} \\
\text{Figure 10: Measurement results}
\end{align*}
\]

\[
P_{av} = P_{ERP} G_r \left(\frac{\lambda}{4\pi d}\right)^2 ,
\]

where \( d \) is the read-out distance, \( G_r \) the gain of the transponder antenna, and \( P_{ERP} \) the ERP-power. The available power is then 108µW, which is higher than the 40µW yielded by the simulation. This discrepancy can be attributed to the mismatch between antenna and chip. We can trace down this error by making use of the power transmission coefficient \( k \) given by

\[
k = \frac{4R_x R_a}{|Z_r + Z_a|} \quad (7)
\]

Here \( R_a \), the (tag) antenna’s radiance resistance, is made four times larger than the real part of the chip input impedance \( R_c \) so as to obtain a relatively large bandwidth. Under this conditions \( k \) is 0.64. The power available for the chip is then 69µW. To further refine the estimation other factors can be considered: the power loss induced by the mismatch between the imaginary part of the tag antenna and the chip, the ohmic loss of the antenna and the loss caused by bond wires and the substrate (PCB).

In Europe, the \( P_{ERP} \) may be as high as 2W. The presented frontend with the employed antenna can then be estimated to operate at a read-out distance of about 5.1m.

V. CONCLUSIONS

An analog frontend for passive UHF/microwave RFID transponders was presented, working under the international standard ISO/IEC 18000-4/6 and supporting all available operating modes. The physical implementation took place on a commercial standard CMOS process with a minimal feature size of 0.35µm. Special RF structures such as Schottky diodes and MIM capacitors are not necessary. The frontend can nominally provide a supply of 1V at 2µA of current consumption. The chip was matched to a resonant antenna of small dimensions (7 x 1.5 cm²). Measurement results coincide largely with those obtained though simulation when losses in the antenna, substrate and wires are considered, thus confirming the effectiveness of the design procedure. A maximum read-out distance of up to 5.1m can be achieved at UHF frequency band under European regulations. The frontend can also operate in the ISM microwave frequency band (2.45GHz) with a somewhat reduced read-out distance.

REFERENCE